CLAIMS

What is claimed is:

1. An apparatus, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache associated with a memory module, the command sequencer and serializer unit to cause a current line of data to be written from the command sequencer and serializer unit to the data cache.

2. The apparatus of claim 1, the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module.

3. The apparatus of claim 2, the command sequencer and serializer to deliver a writeback command to the data cache associated with the memory module, the writeback command to cause the previous line of data stored in the eviction buffer to be written out to a memory module memory device.

4. The apparatus of claim 3, the writeback command including way information and bank address information.

5. An apparatus, comprising:

at least one memory device; and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a memory bus, the memory controller component including an array of tag address storage locations, the memory controller writing a current line of data to the data cache.

6. The apparatus of claim 5, the memory controller further instructing the data cache to evict a previous line of data from the data cache into an eviction buffer.

7. The apparatus of claim 6, the memory controller to deliver a writeback command to the data cache, the writeback command to cause the previous line of data to be written out of the eviction buffer to the memory device.

8. The apparatus of claim 7, the writeback command including way information and bank address information.

9. A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller, the memory module including

at least one memory device, and

a data cache coupled to the memory device, the data cache controlled by a

plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache.

10. The system of claim 9, the memory controller further instructing the data cache to evict a previous line of data from the data cache into an eviction buffer.

11. The system of claim 10, the memory controller to deliver a writeback command to the data cache, the writeback command to cause the previous line of data to be written out of the eviction buffer to the memory device.

12. The system of claim 11, the writeback command including way information and bank address information.

13. A method, comprising:

writing a current line of data from a memory controller to a data cache located on a memory module;

evicting a previous line of data from the data cache to an eviction buffer located on the memory module; and

writing the previous line of data from the eviction buffer to a memory device on the memory module when the memory device is not busy.

14. The method of claim 13, wherein writing the previous line of data from the eviction buffer to the memory device includes receiving a writeback command from a memory controller at the data cache.

15. The method of claim 14, wherein receiving a writeback command includes receiving way information and bank address information.